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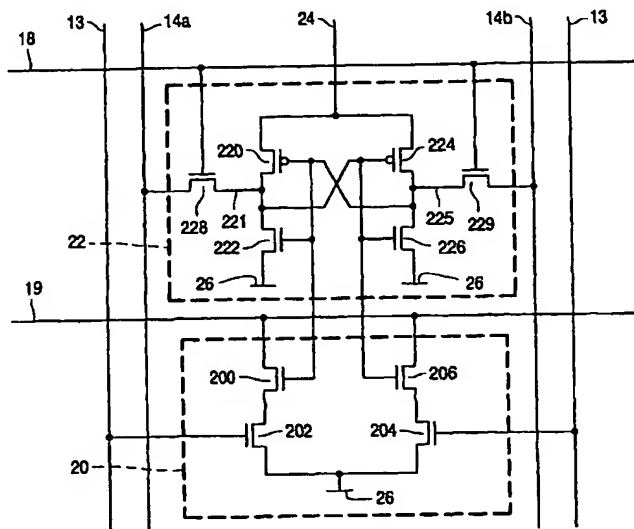
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(54) Title: DEVICE WRITING TO A PLURALITY OF ROWS IN A MEMORY MATRIX SIMULTANEOUSLY



(57) Abstract: A word line driver circuit (10) is coupled to word lines (18) of a memory matrix, for example a matrix of content addressable cells (12). The word line driver circuit is capable of selecting a plurality of word lines simultaneously to permit writing into memory cells in a plurality of rows via the same bit line simultaneously. Cell strength control circuitry (17) reduces a drive strength required to write data into the cells, relative to a drive strength of the bit line driver circuits (15), at least during writing data into memory cells in a plurality of rows of memory cells. Preferably, the drive strength control circuitry (17) contain a resistive element in the power supply lines of the memory cells in a column, so that the supply voltage of the cells in the column is increasingly reduced when more current is drawn during writing of more cells simultaneously.